ABSTRACT

Efficiently implemented multi-channel integrators and multi-channel differentiators utilize a delay section in a single integrator or differentiator in lieu of parallel integrator or differentiator lines to handle multi-channel data flow and processing. The delay section functions like a shift register, greatly reducing the space and/or resources required for implementing the integrator or differentiator. Such integrators and differentiators can be used in multi-channel decimators, interpolators and numerically controlled oscillators in place of multiple instances of single channel integrators that have had to be used in earlier systems. These structures and devices can be implemented in programmable devices such as PLDs and similar devices, in which the delay section can be implemented in embedded memory in the device. Multi-stage decimators and interpolators can use multiple instances of an integrator and/or differentiator in series.